

REMARKS

Drawings

Applicants are submitting herewith a Replacement Sheet which includes Figure 4. The only change Applicants have knowingly made to Figure 4 is to correct the typographical error pointed out by the Examiner. Specifically, Applicants have replaced reference number "78" with reference number "79" between the match circuit and the timer circuit. Applicants thank the Examiner for bringing this typographical error to our attention.

Rejections under 35 U.S.C. 112

Regarding claims 1-10, the Examiner stated that he "assumed that the third signal provided from the first manager is representative of a second domain" (Office Action dated 8/27/03, top of page 3). This is contrary to the express statement in claim 1 that the third signal is "representative of the first domain and a second domain", which is indeed what the invention requires.

The Examiner seems to be adding into the claim text the limitation that the "second value representative of the second domain" was received by the second manager by way of the third signal (which is representative of the first domain and the second domain). It may be this apparent assumption by the Examiner that is causing the confusion. The claim language itself is not confusing. The language of claim 1 places no restrictions on the origin or source of the "second value representative of the second domain". For example, for some embodiments of the claimed invention, the second value could be stored in the second manager, could be derived in the second manager in any manner (e.g. from a value present in the second manager and a clock used to operate the second manager), or could be externally provided to the second manager. Claim 1 in no way limits the manner in which the second value is made available for the second manager. The only limitation expressly made regarding the second value is that it is "representative of the second domain". Note that the third signal is expressly stated to be "representative of the first domain and a second domain". For example, for some embodiments of the claimed invention, the third signal may be used to fully or partially express the relationship between the first domain and the second domain.

Thus, the second manager does indeed operate on the first and second values representative of the first and second domains respectively, in response to the second and third signals. For one embodiment of the present invention, the first value may be representative of a first domain, the second value may be representative of the second domain, and the third signal may be representative of the first domain and the second domain (e.g. a relationship between the first and second domains).

Applicants hope that this explanation clarifies the matter so that prosecution can proceed without the Examiner making assumptions. However, if the Examiner remains unclear "how the second value ... is representative of only the second domain, when the third signal is representative of both the first and second domains" (Office Action dated 8/27/03, bottom of page 2), Applicants would suggest that the Examiner contact us so that we can arrange an Examiner Interview to clarify the matter before the next Office Action.

Rejections under 35 U.S.C. 102 and 103

Regarding claims 1-10, the Examiner stated that he "assumed that the third signal provided from the first manager is representative of a second domain" (Office Action dated 8/27/03, top of page 3). This is contrary to the express statement in claim 1 that the third signal is "representative of the first domain and a second domain", which is indeed what the invention in claims 1-10 requires. Thus all of the Examiner's analysis is based on this faulty assumption. Applicants respectfully assert that none of the prior art of record teaches the claimed invention, including the third signal representative of the first domain and the second domain, wherein the second manager operates in the manner expressly described in claim 1. Claims 2-10 are allowable for at least the same reasons given above.

Claim 11 was rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 3,644,840 (herein referred to as "Connor"). The Examiner asserted that the "add/subtract" logic claimed in claim 11 is taught by the adder in FIG. 1 of Connor. Since the add/subtract logic of claim 11 is "responsive to the first signal", then the only input signal to adder 40 (from register 34) must be what the Examiner is mapping to Applicants' first signal. Claim 11 also requires that the adder be coupled to a register which holds the second signal. The only other signal coupled to adder 40 is the signal from register 36, so the Examiner must be mapping register 36 to the register of claim 11. However, the register 36 and the adder 40 of FIG. 1 in Connor are

coupled so that both are inputs to Af 42. There is no input path illustrated from register 36 to adder 40 of Connor which would allow adder 40 to receive the second signal. And if there is no path by which the second signal can be provided to adder 40 in Connor, then the adder logic 40 cannot "adjust the magnitude of the second signal" as required by claim 11. Applicants respectfully point out that the text of Connor uses the term "network 40" (Connor, col. 4, line 66) and provides no other mention of reference number 40 that Applicant was able to find in regard to FIG. 1. Thus Applicants respectfully assert that the present invention as claimed in claim 11 is not anticipated by Connor. If Applicants have made some incorrect assumptions in the above analysis, Applicants respectfully request clarification. Specifically, (A) which signal is the Examiner interpreting as the first signal?; (B) which signal is the Examiner interpreting as the second signal?; and (C) which register (34 or 36) is the Examiner interpreting as the claimed register?

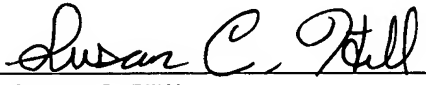
Applicants believe the application is in condition for allowance which action is respectfully solicited. Please contact me if there are any issues regarding this communication or the current Application.

Respectfully submitted,

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